REMARKS/ARGUMENTS

Claims 1-17 are pending in this application. By this amendment, Applicants amend the specification.

Applicants have deleted the first three lines on page 20 of the originally filed specification, as these lines were inadvertently included on page 20.

Claims 1-8, 10, 12 and 13 were rejected under 35 U.S.C. § 102(b) as being anticipated by Hasegawa et al. (U.S. 4,651,344). Claims 9 and 11 were rejected under 35 USC § 103(a) as being unpatentable over Hasegawa et al. in view of Trinh (U.S. 5,265,266). Claims 14-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hasegawa et al. in view of Lee et al. (U.S. 6,483,355). Applicants respectfully traverse these prior art rejections.

Claim 1 recites:

> "A mixer comprising:
> a balun including two balanced lines each having a first end that is short-circuited and a second end that defines a balanced terminal, and an unbalanced line having a first end that is free and a second end that defines an unbalanced terminal;
> a pair of mixer diodes connected to respective ones of the balanced terminals;
> an LO port connected to the unbalanced terminal;
> a high-pass filter;
> **an RF port connected to a node between said mixer diodes through said high-pass filter**;
> a low-pass filter; and
> **an IF port connected to the node between said mixer diodes through said low-pass filter**;
> wherein said balun, said pair of mixer diodes, said high-pass filter, and said low-pass filter are integrated into a multilayer substrate that includes a plurality of sheet layers stacked on each other; and
> **the multilayer substrate has first external terminals that respectively define said LO port, said RF port, and said IF port at the side surfaces thereof, and has second external terminals that define a ground, at least one of the second external terminals being arranged between two of the first external terminals.**" (emphasis added)

With the improved features recited in Applicants' claim 1, including the features of "an RF port connected to a node between said mixer diodes through said high-pass filter," "an IF port connected to the node between said mixer diodes through said low-pass filter" and "the multilayer substrate has first external terminals that respectively define said LO port, said RF port, and said IF port at the side surfaces thereof, and has second external terminals that define a ground, at least one of the second external terminals being arranged between two of the first external terminals," Applicants have been able to provide a mixer that is miniaturized and that prevents degradation of its characteristics (see, for example, the first full paragraph on page 3 of the originally filed specification).

The Examiner alleged that Hasegawa et al. teaches each and every feature recited in claim 1, including an RF port 1 connected to a node between mixer diodes 17, 18 through a high pass filter 20, an IF port 2 connected to the node between the mixer diodes 17, 18 through a low-pass filter 20, and "the multilayer substrate has first external terminals that respectively define said LO port, said RF port, and said IF port at the side surfaces thereof, and has second external terminals that define a ground, at least one of the second external terminals being arranged between two of the first external terminals." Applicants respectfully disagree.

First, contrary to the Examiner's allegations, the RF port 1 of Hasegawa et al. is connected to the **low-pass filter 19**, NOT to a high-pass filter as recited in Applicants' claim 1.

Second contrary to the Examiner's allegations, the IF port 2 of Hasegawa et al. is connected to the **high-pass filter 20**, NOT to a low-pass filter as recited in Applicants' claim 1.

Thus, not only does Hasegawa et al. clearly fail to teach or suggest the features of "an RF port connected to a node between said mixer diodes through said high-pass filter" and "an IF port connected to the node between said mixer diodes through said low-pass filter" as recited in Applicants' claim 1, but Hasegawa et al. actually teaches

the **exact opposite** configuration and arrangement of elements.

Third, contrary to the Examiner's allegations, Hasegawa et al. fails to teach or suggest any specific configuration or arrangement of first and second external terminals on a multilayer substrate, and certainly fails to teach or suggest the features of "the multilayer substrate has first external terminals that respectively define said LO port, said RF port, and said IF port at the side surfaces thereof, and has second external terminals that define a ground, at least one of the second external terminals being arranged between two of the first external terminals" as recited in Applicants' claim 1.

The Examiner alleged that col. 3, lines 32-59, col. 4, lines 48-57, col. 5, lines 44-64 and Figures 4A, 4B, and 5A-5C of Hasegawa et al. teach the specific configuration and arrangement of first and second external terminals as recited in Applicants' claim 1. However, none of these portions of Hasegawa et al., nor any other portion of Hasegawa et al., teaches or suggests **any specific configuration and arrangement** of first and second external terminals on a multilayer substrate. Thus, Hasegawa et al. certainly fails to teach or suggest the features of "the multilayer substrate has first external terminals that respectively define said LO port, said RF port, and said IF port at the side surfaces thereof, and has second external terminals that define a ground, at least one of the second external terminals being arranged between two of the first external terminals" as recited in Applicants' claim 1.

Fourth, the Examiner has clearly improperly relied upon element 20 of Hasegawa et al. to allegedly teach **both** a high-pass filter **and** a low-pass filter. In contrast to the Examiner's allegations, Hasegawa et al. specifically discloses that element 20 is a high-pass filter, and that element 19, **NOT** element 20, is a low-pass filter (see, col. 3, lines 54-59 of Hasegawa et al.).

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 1 under 35 U.S.C. § 102(b) as being anticipated by Hasegawa et al.

The Examiner relied upon Trinh and Lee et al. to allegedly cure various

deficiencies of Hasegawa et al. However, neither Trinh nor Lee et al. teaches or suggests the features of "an RF port connected to a node between said mixer diodes through said high-pass filter," "an IF port connected to the node between said mixer diodes through said low-pass filter" and "the multilayer substrate has first external terminals that respectively define said LO port, said RF port, and said IF port at the side surfaces thereof, and has second external terminals that define a ground, at least one of the second external terminals being arranged between two of the first external terminals" as recited in Applicants' claim 1. Thus, Applicants respectfully submit that Trinh and Lee et al. fail to cure the deficiencies of Hasegawa et al. described above.

Accordingly, Applicants respectfully submit that Hasegawa et al., Trinh and Lee et al., applied alone or in combination, fail to teach or suggest the unique combination and arrangement of elements recited in Applicants' claim 1.

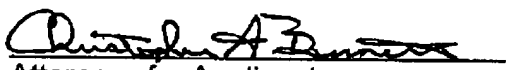
In view of the foregoing amendments and remarks, Applicants respectfully submit that claim 1 is allowable. Claims 2-17 depend upon claim 1, and are therefore allowable for at least the reasons that claim 1 is allowable.

In view of the foregoing amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

Date: October 6, 2004



Attorneys for Applicants

Joseph R. Keating
Registration No. 37,368

Christopher A. Bennett
Registration No. 46,710

KEATING & BENNETT LLP
10400 Eaton Place, Suite 312
Fairfax, VA 22030
Telephone: (703) 385-5200
Facsimile: (703) 385-5080